

Appln No. 09/641,930

Amdt date November 19, 2004

Reply to Office action of July 19, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)
2. (Canceled)
3. (Canceled)
4. (Previously Presented) The system of claim 11 wherein the core transport processor, the first satellite transport processor and the second satellite transport processor are integrated on an integrated circuit chip.
5. (Canceled)
6. (Previously Presented) The system of claim 11 wherein the data related to the compressed data streams include clock reference data.
7. (Canceled)

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8. (Previously Presented) The system of claim 11 wherein said at least one MPEG-2 Transport stream includes at least one in-band stream and at least one out-of-band stream.

9. (Canceled)

10. (Previously Presented) The system of claim 11 further comprising an MPEG-2 video decoder for reading the video data from the memory block and decoding the video data.

11. (Previously Presented)

A system comprising:

a core transport processor for receiving a plurality of compressed data streams;

a first satellite transport processor for receiving at least one of the compressed data streams and extracting video data; and

a second satellite transport processor for receiving at least one of the compressed data streams and extracting audio data,

wherein the core transport processor provides data related to the compressed data streams to at least one of the first satellite transport processor and the second satellite transport processor,

wherein the first satellite transport processor stores the video data in a memory block and generates a start code table to index the video data stored in the memory block,

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wherein the plurality of compressed data streams include at least one MPEG-2 Transport stream, and

wherein the video data includes a plurality of SLICES, and the start code table is used to index the video data, SLICE by SLICE.

12. (Original) The system of claim 11 wherein the plurality of SLICES include a plurality of rows of video data in the memory block, and the start code table is used to index the video data, row by row.

13. (Original) The system of claim 11 wherein the first satellite transport processor aligns the start of each of the plurality of SLICES to a suitable boundary in the memory block when storing the video data in the memory block.

14. (Previously Presented) The system of claim 11 wherein the first satellite transport processor processes down to and including a SLICE layer of said at least one MPEG-2 Transport stream.

15. (Previously Presented) The system of claim 11 wherein the video data includes at least one HDTV video.

16. (Canceled)

17. (Canceled)

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18. (Previously Presented) The method of processing a plurality of transport streams of claim 23 wherein the step of transferring data related to the compressed data streams comprises the step of transferring clock reference data.

19. (Canceled)

20. (Previously Presented) The method of processing a plurality of transport streams of claim 23 wherein the step of receiving at least one MPEG-2 Transport stream comprises the steps of receiving at least one in-band stream and receiving at least one out-of-band stream.

21. (Canceled)

22. (Previously Presented) The method of processing a plurality of transport streams of claim 23 further comprising the steps of reading the video data from the memory block and decoding the video data.

23. (Previously Presented) A method of processing a plurality of transport streams using a system with multiple transport processors comprising the steps of:

receiving a plurality of compressed data streams at a core transport processor;

receiving at least one of the plurality of compressed data streams at a first satellite transport processor, and extracting video data;

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receiving at least one of the plurality of compressed data streams at a second satellite transport processor, and extracting audio data;

transferring data related to the compressed data streams from the core transport processor to at least one of the first satellite transport processor and the second satellite transport processor;

storing the video data in a memory block; and

generating a start code table to index the video data stored in the memory block,

wherein the step of receiving the plurality of compressed data streams comprises the step of receiving at least one MPEG-2 Transport stream, and

wherein the step of reading the video data includes the step of indexing the video data, SLICE by SLICE.

24. (Previously Presented) A method of processing a plurality of transport streams using a system with multiple transport processors comprising the steps of:

receiving a plurality of compressed data streams at a core transport processor;

receiving at least one of the plurality of compressed data streams at a first satellite transport processor, and extracting video data;

receiving at least one of the plurality of compressed data streams at a second satellite transport processor, and extracting audio data;

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transferring data related to the compressed data streams from the core transport processor to at least one of the first satellite transport processor and the second satellite transport processor;

storing the video data in a memory block;

generating a start code table to index the video data stored in the memory block;

reading the video data from the memory block; and

decoding the video data,

wherein the step of receiving the plurality of compressed data streams comprises the step of receiving at least one MPEG-2 Transport stream, and

wherein the video data is stored in the memory block as rows, and the step of reading the video data includes the step of indexing the video data, row by row.

25. (Previously Presented) A method of processing a plurality of transport streams using a system with multiple transport processors comprising the steps of:

receiving a plurality of compressed data streams at a core transport processor;

receiving at least one of the plurality of compressed data streams at a first satellite transport processor, and extracting video data;

receiving at least one of the plurality of compressed data streams at a second satellite transport processor, and extracting audio data;

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transferring data related to the compressed data streams from the core transport processor to at least one of the first satellite transport processor and the second satellite transport processor;

storing the video data in a memory block; and

generating a start code table to index the video data stored in the memory block,

wherein the step of storing the video data comprises the step of aligning a start of each of the plurality of SLICES to a suitable boundary in the memory block.

26. (Previously Presented) The method of processing a plurality of transport streams of claim 23 wherein the step of extracting video data comprises the step of extracting at least one HDTV video.

27. (Previously Presented) A system comprising:

a core transport processor for receiving a plurality of compressed data streams;

a satellite transport processor for receiving at least one of the compressed data streams and for extracting video data, the video data including a plurality of SLICES;

an MPEG-2 video decoder for decoding the video data to generate decoded video data; and

a video compositor for blending the decoded video data with graphics,

wherein the satellite transport processor generates a start code table to index the video data and aligns the

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plurality of SLICES to a suitable boundary in an external memory.

28. (Original) The system of claim 27 wherein the core transport processor, the satellite transport processor, the MPEG-2 video decoder and the video compositor are integrated on an integrated circuit chip.

29. (Original) The system of claim 27 wherein the video data include SDTV video data.

30. (Original) The system of claim 27 wherein the video data include HDTV video data.

31. (Canceled)

32. (Currently Amended) ~~The video transport processor of claim 31, further comprising~~ A video transport processor comprising:

an input for receiving an MPEG Transport stream including MPEG video data comprising a plurality of SLICES;

a transport processor for processing headers in the MPEG Transport stream;

a start code alignment module for storing the MPEG video data in an external memory, for aligning a start of the plurality of SLICES to a suitable boundary in the external memory when storing the MPEG video data in the external memory,

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and for generating a start code table to index the MPEG video data stored in the external memory; and

a switch for providing the MPEG Transport stream to the transport processor or the start code alignment module.

33. (Previously Presented) The video transport processor of claim 32, wherein the switch provides the MPEG Transport stream first to the transport processor, and provides the MPEG Transport stream to the start code alignment module after one or more headers have been processed.

34. (Canceled)

35. (Canceled)

36. (Currently Amended) ~~The video transport processor of claim 31,~~ A video transport processor comprising:

an input for receiving an MPEG Transport stream including MPEG video data comprising a plurality of SLICES;

a transport processor for processing headers in the MPEG Transport stream; and

a start code alignment module for storing the MPEG video data in an external memory, for aligning a start of the plurality of SLICES to a suitable boundary in the external memory when storing the MPEG video data in the external memory, and for generating a start code table to index the MPEG video data stored in the external memory,

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wherein one or more zeros are added to at least one of the SLICES to align another one of the SLICES to the suitable boundary in the external memory.